

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Application No.		
				MIC-12693-1P US		Filed Herewith		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				Applicant(s)		Confirmation No.		
				Shekar Mallikarjunaswamy		Unknown		
				Filing Date		Group		
				Filed Herewith		Unknown		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
<i>QWg</i>	AA	4,109,274	8/22/1978	Belenkov et al.	357	38		
	AB	4,605,980	8/12/1986	Hartranft et al.	361	56		
	AC	4,745,450	5/17/1988	Hartranft et al.	357	23.13		
	AD	4,807,080	2/21/1989	Clark	361	56		
	AE	5,162,888	11/10/1992	Co et al.	257	408		
	AF	5,424,226	6/13/1995	Vo et al.	437	30		
	AG	5,504,444	4/2/1996	Neugebauer	327	108		
	AH	5,537,075	7/16/1996	Miyazaki	327	566		
	AI	5,571,737	11/5/1996	Sheu et al.	437	44		
	AJ	5,578,860	11/26/1996	Costa et al.	257	528		
	AK	5,602,404	2/11/1997	Chen et al.	257	112		
	AL	5,753,920	5/19/1998	Buehler et al.	250	370.06		
	AM	5,844,280	12/1/1998	Kim	257	355		
	AN	5,870,268	2/9/1999	Lin et al.	361	111		
<i>QWg</i>	AO	6,064,249	5/16/2000	Duvvury et al.	327	314		
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
<i>QWg</i>	AL	WO 96/30936	3-Oct-1996	PCT				
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
<i>QWg</i>	AQ	Antinone, Robert J. et al., "Electrical Overstress Protection For Electronic Devices," Noyes Publications, pages 17-26.						
<i>QWg</i>	AR	Pendharkar, Sameer et al., "SCR-LDMOS - A Novel LDMOS Device With ESD Robustness," 2000 IEEE, pages 341-344.						
<i>QWg</i>		Wang, Albert Z.H. et al., "An On-Chip ESD Protection Circuit with Low Trigger Voltage in BiCMOS Technology," IEEE Journal of Solid-State Circuits, Vol. 36, No. 1, January 2001, pages 40-45.						
Examiner <i>QWg</i>	Date Considered	11/8/04						
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		AO						
		AP						

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<i>DWG</i>	AQ	Antinone, Robert J. et al., "Electrical Overstress Protection For Electronic Devices," Park Ridge, N.J., U.S.A.: Noyes Publications, 1986, pages 17-26.						
<i>DWG</i>	AR	Iwamuro, N. et al., "Switching Loss Analysis Of Shorted Drain Non Punch-Through And Punch-Through Type IGBTs In Voltage Resonant Circuit," 3 <sup>rd</sup> International Symposium on Power Semiconductor Devices and ICS, ISPSD '91, April 22-24, 1991, pages 220-225.						
<i>DWG</i>	AS	Simpson, M. R. et al., "Analysis Of The Lateral Insulated Gate Transistor," International Electron Devices meeting, Washington, D.C., December 1-4, 1985, pages 740-743.						

Examiner *Douglas A. Green* Date Considered *11/8/04*

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Substitute for form 1449A/PTO FEB 02 2004		Application Number	10/665,806
		Filing Date	9/19/2003
		First Named Inventor:	MALLIKARJUNASWAMY, Shekar
		Examiner name: Unknown	GROUP: 2811
Sheet	1	of	2
Attorney Docket Number MIC-12693-1P			

## U.S. PATENT DOCUMENTS

Examiner Initials*	Cited No. <sup>1</sup>	Document Number Number - Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Figures Appear
RKg		US-5,374,844	12/1994	Moyer	
		US-5,528,188	06/1996	Au et al.	
		US-5,546,038	08/1996	Croft	
		US-5,631,793	05/1997	Ker et al.	
		US-5,959,488	09/1999	Lin et al.	
		US-6,013,942	01/2000	Soderbarg et al.	
		US-6,064,109	05/2000	Blanchard et al.	
		US-6,097,235	08/2000	Hsu et al.	
		US-6,194,764	B1 02/2001	Gossner et al.	
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		US-6,320,232	B1 11/2001	Gossner et al.	
RKg		US-6,414,532	B1 07/2002	Su et al.	

## FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document Cntry Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Figures Appear	T <sup>6</sup>

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

RKg	Charvaka Duvvury et al. "Substrate Pump NMOS for ESD Protection Applications," Silicon Technology Development, Texas Instruments, Dallas, Texas, 11 pages.

EXAMINER SIGNATURE: <i>Douglas K. Powers</i>	DATE CONSIDERED: 11/8/04
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DW9		US-6,437,419	B1 08/2002	Bhalla et al.	
DW9		US-6,469,560	B1 10/2002	Chang et al.	
DW9		US-6,507,471	B2 01/2003	Colclaser et al.	
<b>FOREIGN PATENT DOCUMENTS</b>					
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document Cntry Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5/known</sup>	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Passages or Figures Appear
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>					
EXAMINER SIGNATURE: <i>Douglas W. Owen</i>			DATE CONSIDERED: 11/8/04		

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